

This Page Is Inserted by IFW Operations
and is not a part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

**As rescanning documents *will not* correct images,
please do not report the images to the
Image Problem Mailbox.**

REMARKS

The Office Action mailed November 7, 2001, has been received and reviewed. Claims 1 through 9 are currently pending in the application. Claims 1 through 9 stand rejected. Applicant has amended claims 1 through 9 and respectfully request reconsideration of the application as amended herein.

Information Disclosure Statement

Applicant notes the filing of an Information Disclosure Statement herein on August 25, 2000 and a Supplemental Information Disclosure Statement on November 13, 2001 and notes that no copies of the PTO-1449's were returned with the outstanding Office Action. Applicant respectfully requests that the information cited on these PTO-1449's (which are the same as that of record to that date in the parent application hereto) be made of record herein.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on U.S. Patent No. 4,943,539 to Wilson et al.

Independent claims 1, 2, 5, and 6 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Wilson et al. (U.S. Patent 4,943,539). Applicant respectfully traverses this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations**. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

Wilson discloses a two-step etching process for making a multilayer metallization structure. A first interconnect layer 12 is formed on a dielectric layer 11. The first interconnect layer 12 is

covered by a first metal layer 13 which is then covered by a sacrificial layer 14. (Wilson, col. 3, lines 49-51). Preferably, the first interconnect layer comprises aluminum copper alloy, the first metal layer 13 comprises TiW or TiSi and sacrificial layer 14 comprises aluminum alloy or titanium nitride. (*Id.*, col. 3, lines 53-57; col. 4, lines 4-5). The layers 12, 13, 14 are patterned and an interlayer dielectric 16 is formed thereover. (Wilson, FIG. 2). The dielectric layer 16 is patterned and dry etched to expose the sacrificial layer 14. (*Id.* col. 4, lines 17-24; FIG. 3). A second *isotropic* etch, preferably comprising a solution of nitric acid, phosphoric acid, and acetic acid, is then performed. (*Id.* col. 4, lines 34-38). The isotropic etch removes residual backspattered material 19 and etches sacrificial layer 14 in both a downward and sideways direction to create a single “T” shaped void. (*Cf.* Wilson, FIGs. 3 and 4). Additionally, the wet etch chemical “removes residual backspattered material incorporated into the polymer film” (*Id.* at lines 51-55).

Independent claims 1, 2, 5 and 6, as amended, each include similar limitations of an opening “extending from an upper surface of said dielectric layer to a metal-containing conductive pad” and “having substantially parallel sidewalls”. Applicant respectfully submits that figures of the present application depicts openings having substantially parallel sidewalls. Further, the specification teaches forming openings by anisotropic etching. See, for example, specification at page 2, lines 15-25.

Applicant respectfully submits that Wilson fails to teach or suggest an opening in a dielectric layer formed by anisotropic etching having substantially parallel sidewalls. Instead, Wilson expressly teaches a dry etch and an isotropic etch to create a “T” shaped void. (Wilson, col. 4, lines 19-21 and 34-36). As Wilson fails to teach or suggest every limitation of the presently claimed invention, applicant respectfully submits that independent claims 1, 2, 5 and 6 as amended, are not rendered obvious by Wilson. Accordingly, applicant submits that claims 1, 2, 5 and 6 are allowable over Wilson.

Applicant further respectfully submits that the process taught by Wilson et al. would not result in a contact within a residue-free opening or a residue-free contact opening as recited by the claims of the presently claimed invention. Though its true that Wilson et al. teaches the wet isotropic

etch process removes “residual backsputtered material that may have been incorporated in polymer film” (Wilson, col. 4, lines 51-52), Wilson et al. does not teach that the wet etch chemical removes the polymer film itself. Furthermore, the isotropic etch step is used to substantially remove the sacrificial metal layer and create a contact interface with a wider cross section. However, the process of Wilson et al. does not include a cleaning step following the isotropic etch. Thus, any residue created by the isotropic etch step will be left in the contact opening, compromising the performance and durability of the contact ultimately deposited therein. Applicant respectfully submits that the processes of Wilson et al. will not render a contact within a residue-free opening or a residue-free contact opening, and applicant respectfully requests that the rejection of claims 1 through 2 and 5 through 6 be withdrawn.

Obviousness Rejection Based on U.S. Patent No. 4,700,465 to Sirkin

Claims 1 through 9 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Sirkin (U.S. Patent 4,700,465). Applicant respectfully traverses this rejection, as hereinafter set forth.

Sirkin discloses a method of selectively making contact structures both with barrier metal and without barrier metal in a single process. The disclosed process includes providing a silicon substrate 10 underlying a silicon oxide insulating layer. The silicon oxide layer 12 is etched and the silicon substrate 10 is doped with ion to create amorphotized regions 20.


Applicant respectfully submits that Sirkin fails to teach or suggest every limitation of independent claims 1 through 9 as amended. Independent claims 1 through 9, as amended, each recite “a semiconductor substrate having a metal-containing conductive pad” or “said residue-free contact opening extending from an upper surface of said dielectric layer to a metal-containing conductive pad.” By way of contrast, Sirkin teaches forming amorphotized regions 20 by ion implantation and lacks any disclosure of a metal-containing conductive pad. (Sirkin, col. 2, lines 53-58 and col. 3, lines 36-43). As Sirkin fails to teach every limitation of the presently claimed invention, applicant respectfully submits independent claims 1 through 9 of the presently claimed

invention are not obvious in view of Sirkin. Reconsideration and withdrawal of the rejection is requested.

CONCLUSION

Claims 1 through 9 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicant's undersigned attorney.

Respectfully Submitted,



Krista Weber Powell
Registration Number 47,867
Attorney for Applicant
TRASKBRITT, PC
P.O. Box 2550
Salt Lake City, Utah 84110
Telephone: (801) 532-1922

KWP/hlg:dlm

Date: January 3, 2002

Enclosure: Version With Markings to Show Changes Made

N:\2269\3361.2\Amendment.wpd

VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (Twice amended) A residue-free contact opening in a dielectric layer for a semiconductor device extending from an upper surface of said dielectric layer to a metal-containing conductive pad, having substantially parallel sidewalls and formed by a method comprising:
providing a semiconductor substrate having a metal-containing conductive pad;
forming said dielectric layer over said semiconductor substrate and said metal-containing conductive pad with at least one opening extending from an upper surface of said dielectric layer to said metal-containing conductive pad and including a residue residing within said at least one opening;
applying nitric acid within said at least one opening; and
subsequently applying a phosphoric acid-containing solution within said at least one opening.

2. (Twice amended) A contact within a residue-free opening in a dielectric layer for a semiconductor device extending from an upper surface of said dielectric layer to a metal-containing conductive pad, having substantially parallel sidewalls and formed by a method comprising:
providing a semiconductor substrate having a metal-containing conductive pad;
forming said dielectric layer over said semiconductor substrate and said metal-containing conductive pad with at least one opening extending from an upper surface of said dielectric layer to said metal-containing conductive pad, and wherein a residue resides within said at least one opening;
applying a nitric acid within said at least one opening;
subsequently applying a phosphoric acid-containing solution within said at least one opening;
and
disposing conductive material within said at least one opening.

3. (Twice amended) A residue-free contact opening in a dielectric layer and a barrier layer for a semiconductor device comprising a semiconductor substrate having a metal-containing conductive pad under said dielectric layer and said barrier layer, said residue-free contact formed by a method comprising:

providing a semiconductor substrate having a metal-containing conductive pad;

forming said barrier layer over said semiconductor substrate and said metal-containing conductive pad;

forming said dielectric layer over said barrier layer;

forming a first via portion through said dielectric layer to expose a portion of said barrier layer, said formation of said first via portion forming an oxide polymer residue within said first via portion;

forming a second via portion through said exposed portion of said barrier layer, said formation of said second via portion forming a metal polymer residue within said first and second via portions;

applying nitric acid within said first and second via portions to remove said metal polymer residue; and

subsequently applying a phosphoric acid-containing solution within said first via portion to remove said oxide polymer residue.

4. (Twice amended) A residue-free contact opening in a dielectric layer and a barrier layer above a metal-containing conductive pad for a semiconductor device, said residue-free contact formed by a method comprising:

providing a semiconductor substrate having a metal-containing conductive pad;

forming said barrier layer over said semiconductor substrate and said metal-containing conductive pad;

forming said dielectric layer over said barrier layer;

forming a first via portion through said dielectric layer to expose a portion of said barrier layer, said formation of said first via portion forming an oxide polymer residue within said first via portion;

applying a phosphoric acid-containing solution within said first via portion to remove said oxide polymer residue;

forming a second via portion through said exposed portion of said barrier layer, said formation of said second via portion forming a metal polymer residue within said first and second via portions; and

applying a nitric acid-containing solution within said first and second via portions to remove said metal polymer residue.

5. (Twice amended) A residue-free contact opening in a dielectric layer for a semiconductor device extending from an upper surface of said dielectric layer to said metal-containing conductive pad, having substantially parallel sidewalls and formed by a method comprising:

providing a semiconductor substrate having a metal-containing conductive pad;

forming said dielectric layer over said semiconductor substrate and said metal-containing conductive pad with at least one opening extending from an upper surface of said dielectric layer to said metal-containing conductive pad, and wherein a residue resides within said at least one opening;

applying nitric acid within said at least one opening; and

subsequently applying a phosphoric acid solution including a fluorine-containing component within said at least one opening.

6. (Twice amended) A contact within a residue-free opening in a dielectric layer for a semiconductor device extending from an upper surface of said dielectric layer to a metal-containing conductive pad, having substantially parallel sidewalls and formed by a method comprising:

providing a semiconductor substrate having a metal-containing conductive pad;
forming said dielectric layer over said semiconductor substrate and said metal-containing conductive pad with at least one opening extending from an upper surface of said dielectric layer to said metal-containing conductive pad, and wherein a residue resides within said at least one opening;
applying a nitric acid within said at least one opening;
subsequently applying a phosphoric acid solution, including a fluorine-containing component, within said at least one opening; and
disposing conductive material within said at least one opening.

7. (Twice amended) A method of fabricating a contact opening in a dielectric layer and a barrier layer for a semiconductor device, comprising:

providing a semiconductor substrate having a metal-containing conductive pad;
forming said barrier layer over said semiconductor substrate and said metal-containing conductive pad;
forming said dielectric layer over said barrier layer;
forming a first via portion through said dielectric layer to expose a portion of said barrier layer, said formation of said first via portion forming an oxide polymer residue within said first via portion;
forming a second via portion through said exposed portion of said barrier layer, said formation of said second via portion forming a metal polymer residue;
applying nitric acid within said first and second via portions to remove said metal polymer residue; and

subsequently applying a phosphoric acid solution including a fluorine-containing component within said first via portion to remove said oxide polymer residue.

8. (Twice amended) A residue-free contact opening in a dielectric layer and a barrier layer for a semiconductor device including a semiconductor substrate having a metal-containing conductive pad under said dielectric layer and said barrier layer, said residue-free contact formed by a method comprising:

providing a semiconductor substrate having a metal-containing conductive pad;

forming said barrier layer over said semiconductor substrate and said metal-containing conductive pad;

forming said dielectric layer over said barrier layer;

forming a first via portion through said dielectric layer to expose a portion of said barrier layer, said formation of said first via portion forming an oxide polymer residue within said first via portion;

forming a second via portion through said exposed portion of said barrier layer, said formation of said second via portion forming a metal polymer residue within said first and second via portions;

applying nitric acid within said first and second via portions to remove said metal polymer residue; and

subsequently applying a phosphoric acid solution including a fluorine-containing component within said first via portion to remove said oxide polymer residue.

9. (Twice amended) A residue-free contact opening in a dielectric layer and a barrier layer above a metal-containing conductive pad for a semiconductor device, said residue-free contact formed by a method comprising:

providing a semiconductor substrate having a metal-containing conductive pad;

forming said barrier layer over said semiconductor substrate and said metal-containing conductive pad;

forming said dielectric layer over said barrier layer;

forming a first via portion through said dielectric layer to expose a portion of said barrier layer, said formation of said first via portion forming an oxide polymer residue within said first via portion;

applying a solution including a fluorine-containing component within said first via portion to remove said oxide polymer residue;

forming a second via portion through said exposed portion of said barrier layer, said formation of said second via portion forming a metal polymer residue within said first and second via portions; and

applying nitric acid within said first and second via portions to remove said metal polymer residue.